SEMESTER S6

SEMICONDUCTOR PACKAGING AND TESTING

Course Code	**PEEVT 637**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCECT302 Solid State Devices	**Course Type**	Elective

Course Objectives:

1. Understand the various semiconductor packaging techniques, including hermetic and plastic packaging, wire bonding, and flip-chip processes, as well as package form factors and standardizations.
2. Learn the principles and challenges of surface-mount technology, including the comparison of peripheral leads versus area array packages, and explore current and future trends in lead-free and halogen-free packaging.
3. Explore the packaging requirements for various applications, such as MEMS, image sensors, memory cards, and solar technology, and understand the role of copper interconnects and low-k dielectric materials in future packaging options.
4. Gain knowledge of reliability testing methodologies for semiconductor packages, including preconditioning, temperature cycling, thermal shock, and the limitations of current reliability testing techniques.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Semiconductor packaging: Introduction, Hermetic packaging, Plastic packaging, Wire bonding process flow, flip-chip process flow comparison, Equipment, Material interactions. Package form factors and families: Introduction, Package outline standardization, Leaded package families, Quad lead package family, Substrate-based package families, Chip scale packages, Stacked-die package, Package-on-package, Flip-chip packages, Wafer-level chip scale packages.	**9**

2	Surface-mount technology: Objectives, Introduction, Package cracking, Surface-mount packages: peripheral leads versus area array, Issues with advanced packaging, Current and future trends: Lead-free and halogen-free packaging.	**9**
3	Packaging needs: Introduction, Tape automated bonding, Micro electro-mechanical systems (MEMS), Package types used for MEMS, MEMS packaging examples, Image sensor modules, Memory cards, Packaging needs for solar technology. Copper interconnects and low-k dielectric materials. Dielectric constant requirements at each technology node. Future interconnect and dielectric materials. Future packaging options.	**9**
4	Package reliability: Reliability testing – Introduction, Background, Examples of reliability tests: Preconditioning, Package failure mode, Temperature cycling and thermal shock, High-temperature storage life, Temperature-humidity-bias tests, Limitations of reliability testing.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe and differentiate various semiconductor packaging techniques and identify package form factors and standardizations.	**K2**
CO2	Understand the principles of surface-mount technology, identify the challenges of advanced packaging, and recognize trends in lead-free and halogen-free packaging.	**K2**
CO3	Explain the packaging requirements for MEMS, image sensors, memory cards, and solar technology, and understand the importance of copper interconnects and low-k dielectric materials in future packaging solutions.	**K2**
CO4	Conduct and interpret various reliability tests for semiconductor packages, and understand the limitations and significance of these tests in ensuring package reliability.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**1**	**1**	**1**	**1**	**1**				**2**	**1**		**1**
CO2	**2**	**1**	**1**	**1**	**2**				**2**	**1**		**1**
CO3	**2**	**1**	**1**	**1**	**2**				**2**	**2**		**2**
CO4	**2**	**2**	**1**	**2**	**3**				**2**	**2**		**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Semiconductor Packaging – Materials Interaction and Reliability	Andrea Chen, Randy Hsiao-Yu Lo	CRC Press , Taylor & Francis Group	2012
2	Semiconductor Advanced Packaging.	John H Lau	Springer	2021
3	Microelectronic Packaging	Tummala, Rao R.	Springer	2001
4	Electronic Packaging and Interconnection Handbook	Charles A Harper	McGraw-Hill Professional	4th, 2004

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Advanced Electronic Packaging	Richard K. Ulrich, William D. Brown	Wiley-Interscience	2nd Edition, 2006
2	Chip Scale Package	John H. Lau, Ricky S.W. Lee	McGraw-Hill	2002
3	Electronic Packaging, Microelectronics, and Interconnection Dictionary	Charles Harper, Martin Miller	McGraw-Hill Education	2005

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/noc/courses/noc22/SEM1/noc22-me61/
2	https://archive.nptel.ac.in/courses/108/108/108108031/
3	https://www.youtube.com/watch?v=RpLnIiegXbg
4	https://www.youtube.com/watch?v=k2CognMJ_9I